AF/2814

PATENT

Case Docket No. MICRON.061DV1
Date: March 19, 2001

In re application of	:	Ahmad
App. No.	:	09/397,952
Filed	:	September 17, 1999
For	:	FABRICATION OF INTEGRATED DEVICES USING NITROGEN IMPLANTATION
Examiner	:	Stephen H. Rao
Art Unit	:	2814

I hereby certify that this correspondence and all marked attachments are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on

March 19, 2001
(Date)

Adeel S. Akhtar, Reg. No. 41,349

ASSISTANT COMMISSIONER FOR PATENTS BOX AF
WASHINGTON, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below:

CLAIMS AS FILED

	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
Total Claims	21	—	21	= 0 ×	$18	= $0
Independent Claims	4	—	4	= 0 ×	$80	= $0
If application has been amended to contain multiple dependent claim(s), then add					$270	= $0
Time Extension Fee						$0
				TOTAL ADDITIONAL FEE FOR THIS AMENDMENT		$0

(X) Return prepaid postcard.

(X) Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410. A duplicate copy of this sheet is enclosed.

Adeel S. Akhtar
Registration No. 41,349
Attorney of Record

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MICRON.061DV1 PATENT

7-26-01 Payton

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Ahmad	Group Art Unit 2814
Appl. No.	:	09/397,952	
Filed	:	September 17, 1999	
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AMENDMENT AND RESPONSE TO OFFICE ACTION

Assistant Commissioner for Patents
Washington, D.C. 20231
ATTENTION BOX: AF

Dear Sir:

In response to the Office Action mailed January 18, 2001 in the above-captioned application, Applicant respectfully requests entry of the amendments and reconsideration of the claims in view of the remarks below.

In the Claims:

Please amend Claim 1 as follows:

Sub D1

1. (Twice Amended) A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

forming an insulator element region directly on said substrate; and

C1